REMARKS

Claims 1-10, 15-22, and 24-30 are pending in the application. Claims 15-22 and 24-30 are presently allowed. Claims 12-14 and 23 have been canceled by this amendment without prejudice.

Claim 1 has been amended to recite that the first and second instruction buffers are configured to hold a first or second instruction including a dependency indicator and being associated with a first or second thread and that the instruction control unit is configured to detect the dependency indicators and change the value of the dependency counter in response to detecting the dependency indicators and configured to disallow execution of the first instruction if the dependency counter includes a value less than a threshold value. Support for this amendment is found in claim 24.

Claim 7 has been amended to recite that the first instruction and the second instruction include one or more instruction dependency bits and that the dependency counter is incremented and decremented in response to detecting the instruction dependency bits, said instruction control unit configured to disallow execution of the first instruction if said dependency counter includes a value less than a threshold value. Support for this amendment is found in claim 24.

None of the amendments add limitations that were not previously found in the claims.

Claim Rejections – 35 U.S.C. § 102

Claims 1-14 and 23 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Akkary et al., US 6,182,210.

Akkary discloses a method and apparatus for processing dependent threads using predictive methods.

Claim 1 is to an apparatus for instruction-level parallelism in a processing element, comprising: an instruction control unit; a first instruction buffer; a second instruction buffer; a dependency counter; an execution switch; and an execution unit. The first and second instruction buffers are configured to hold first or second instructions including dependency indicators and being associated with a first or second thread. The instruction control unit is configured to detect the dependency indicators and change the value of the dependency counter in response to detecting the dependency indicators and to disallow execution of the first instruction if the dependency counter includes a value less than a threshold value.

Claim 7 is to an apparatus for processing instructions in multiple threads comprising an instruction buffer, a dependency counter, an instruction control unit, and an execution switch. The instruction control unit detects instruction dependency bits and increments and decrements the dependency counter. The first and second instructions include one or more instruction dependency bits. The dependency counter is incremented and decremented in response to detecting the instruction dependency bits and is configured to disallow execution of the first instruction if the dependency counter includes a value less than a threshold value.

In the office action of 12/23/2004, the Examiner stated that claim 24 was allowable based on the limitation that the instruction control unit is configured to disallow execution of the first instruction if the dependency counter value is less than a threshold value. By this amendment, this limitation is incorporated into claims 1 and 7, with required antecedents, thus obviating the rejection.

Claims 2-6 and 8-10 depend from and contain all the limitations of claims 1 and 7 respectively, and are asserted to distinguish from the reference in the same manner as claims 1 and 7.

Claims 12-14 and 23 have been canceled without prejudice.

In view of the foregoing, it is submitted that the application is now in condition for allowance.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

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